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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,015	10/31/2003	Yoshinori Shizuno	OHG 140	8235

23995 7590 11/17/2004

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,015	SHIZUNO, YOSHINORI	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *9-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 7* is/are rejected.

7)☒ Claim(s) *5 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of Group I, claims 1-8, in Paper No. 3 is acknowledged.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

A. Claim 5 recites the limitations "a thin oxidation layer formed on the top surface of said electrode posts".

Therefore, the thin oxidation layer must be shown, or the feature(s) canceled from the claim(s). No new matter should be entered.

B. Claim 8 recites the limitations "a portions of said wiring patterns on a boundary and vicinity thereof between a region on the upper side of said semiconductor chip and the base frame are formed wider or more thickly than other portions of said wiring patterns".

Therefore, the wiring patterns must be shown having wider/thicker pattern in the vicinity of the chip compared to other portions, or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should

include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 5 is objected to because of the following informalities:

The limitations as recited in claim 5 include: ""a thin oxidation layer formed on the top surface of said electrode posts".

However, the description of the embodiment I or the figures in the specification do not disclose such oxidation layer on the top surface of the electrode posts 46.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Ma et al. (US Pat. 6271469)

Regarding claim 1, Ma et al. teach a semiconductor device comprising:

- a support/base frame (see 112 in Fig. 6e) having a first surface and a second surface which opposes the first surface, and having a semiconductor chip/chips in opening portions through formed in the base frame (see 102 in Fig. 6d/6e)
- the chip which has first main surface on which a plurality of contact/electrode pads (not shown in Fig. 6e; see 108 in Fig. 1c-1i; Col. 3, line 40) are provided and a second main surface opposing said first main surface, and which disposed within said opening portion such that the level of the first main surface is substantially equal to the level of the first surface (see Fig. 6d)
- an insulating/dielectric film (see 118 in Fig. 6e) formed on the first surface and the first main surface such that a portion/part of each of the plurality of electrode pads is exposed for wiring connections

- a plurality of wiring patterns/conductive traces/conductive plugs (see 124/132 in Fig. 6e) which are electrically connected to the plurality of electrode pads, respectively and which extend from said electrode pads to the upper side of the first surface of the base frame
- an insulating dielectric/sealing portion (see 126 in Fig. 6e) formed on the insulating/dielectric film such that a part of each of the wiring patterns/conductive traces/conductive plugs is exposed, and
- a plurality of external pads/terminals (134 in Fig. 6e) provided over the wiring patterns/conductive traces in a region including the upper side of the support/base frame

(Fig. 6e; 6a-6e; Col. 7, lines 12-42; Col. 1-4).

Regarding claims 3 and 4, Ma et al. disclose the entire claimed structure as applied to claim 1 above, wherein Ma et al. disclose the wiring patterns/conductive traces/conductive plugs (see 124/132 in Fig. 6e) comprising a plurality of conductive plugs/posts (see 132 in Fig. 6e) formed between the wiring patterns and the external pads/terminals wherein the insulating dielectric/sealing portion is formed such that a top surface the electrode plugs/posts is exposed and the conductive plugs/posts being made of a conductive material (see Fig. 1i; Col. 5, lines 12-15).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

7. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (US Pat. 6271469).

Regarding claim 2, Ma et al. teach substantially the entire claimed structure as applied to claim 1 above, except the external terminals being arranged at a first pitch wider than a second pitch at which the electrode pads are arranged.

Ma et al. further teach another embodiment (Fig. 1j) where a first pitch of the external bumps/terminals is wider/larger than a second pitch of the chip electrode pads (see arrangement of 138 and 108 in Fig. 1j; Col. 3, line 30- Col. 5, line 30).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the external terminals being arranged at a first pitch wider than a second pitch at which the electrode pads are arranged as taught by the embodiment in Fig. 1j in Ma et al. so that shorting of the external terminals can be prevented in Ma et al's device.

Regarding claim 6, Ma et al. teach substantially the entire claimed structure as applied to claim 1 above, except a lower base for supporting the second main surface of the chip and the second surface of the base frame.

Ma et al. further teach another embodiment (Fig. 7e) where a plurality of lower bases/substrates are incorporated in the structure to support the second main surface of the chip and the second surface of the support/base frame (see 152 and 162 respectively in Fig. 7e) and to improve thermal performance (Col. 7, lines 42-66).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the lower base for supporting the second main surface of the chip and the second surface of the base frame as taught by the embodiment in Fig. 7e in Ma et al. so that the thermal performance and the rigidity can be improved in Ma et al/s device.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (US Pat. 6271469) in view of Fukutomi et al. (US Pat. 6268648).

Regarding claim 7, Ma et al. teach substantially the entire claimed structure as applied to claim 1 above, except the base frame comprising inside walls which define the opening portion, thickness of the inside walls gradually decreasing toward the chip.

Fukutomi et al. teach a device package having a base substrate/frame (see Fig. 1) having a through opening with a cavity where the base substrate/frame comprises

inside walls having a ramp/inclined surface which define the opening portion, thickness of the inside walls gradually decreases towards the chip (see Fig. 1; Col. 7, lines 1-20).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the base frame comprising inside walls which define the opening portion, thickness of the inside walls gradually decreasing toward the chip as taught by Fukutomi et al. so that the adhesion and rigidity can be improved and thermal stress can be reduced in Ma et al's device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

NITIN PAREKH

11-15-04

PATENT EXAMINER

Technology Center 2800